Lazy x86-TSO Memory Model for C++ Verification

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Verification of Parallel Programs I

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- easy to make mistakes – data races, deadlocks

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- is it possible to end with `a == 0 && b == 0`? **yes**

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- program is translated into LLVM intermediate language
- LLVM is executed by the model checker
- exploration of ~~all possible~~ runs of the program
  - actually of some representants of classes of equivalent runs
- detect assertions, memory errors, compiler traps, ...

Relaxed Memory Example

```
int x, y = 0;
void thread0() {
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void thread1() {
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memory

x	0
y	0

thread 0

```
y = 1;
load x;
```

store buffer of t. 0

thread 1

```
x = 1;
load y;
load x;
```

store buffer of t. 1

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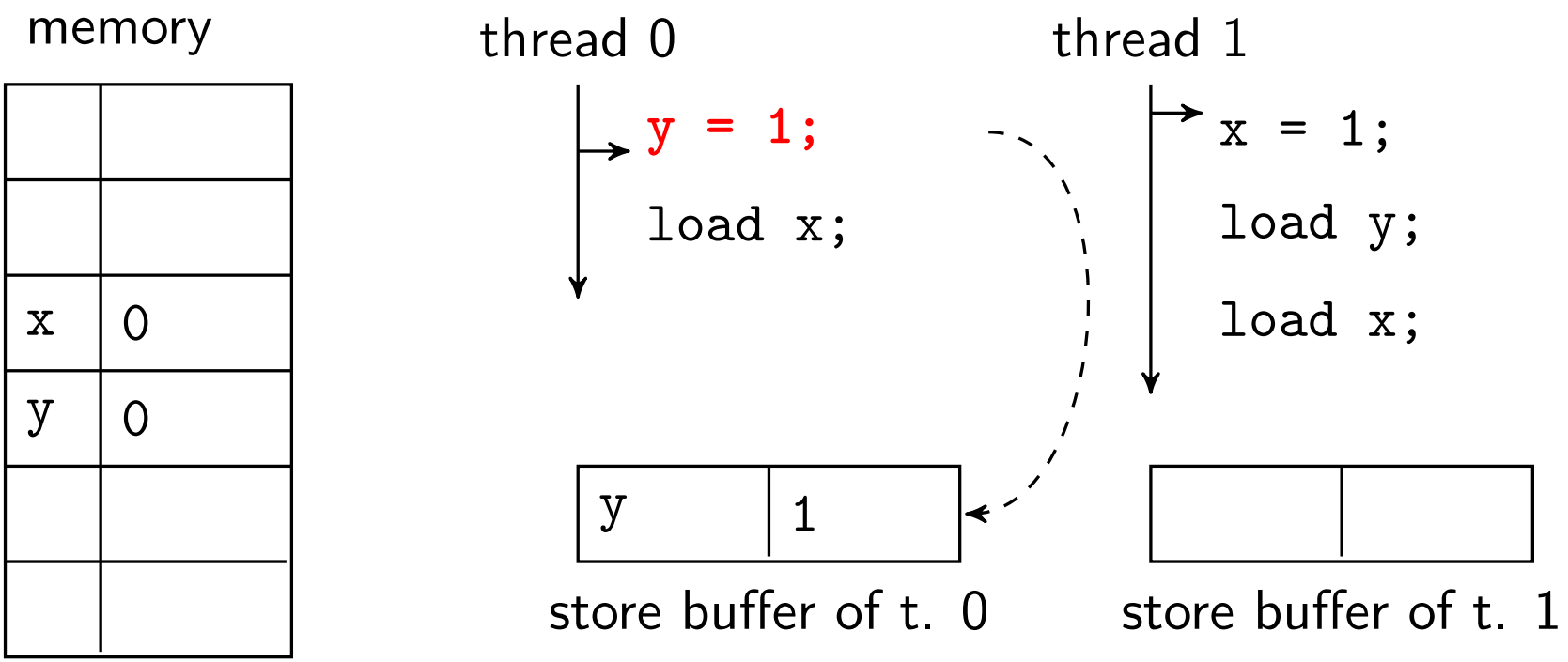

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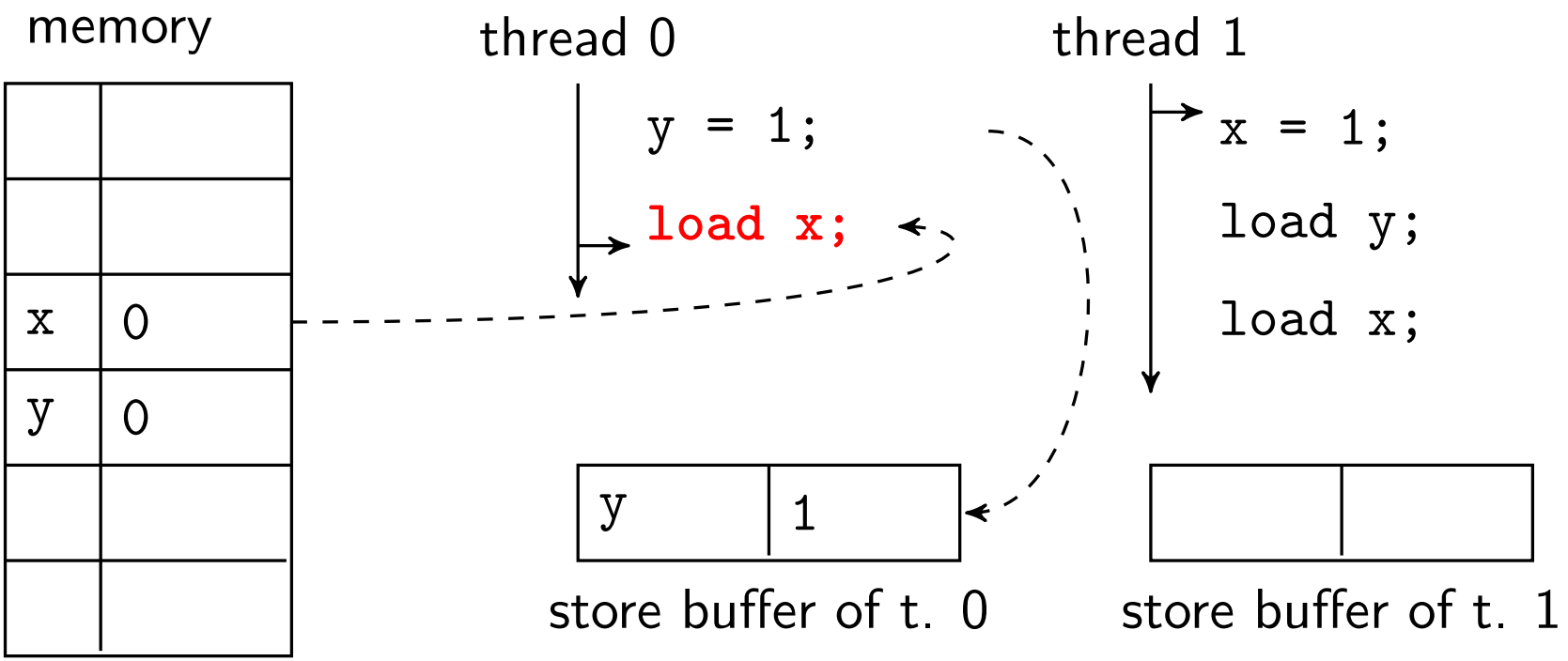

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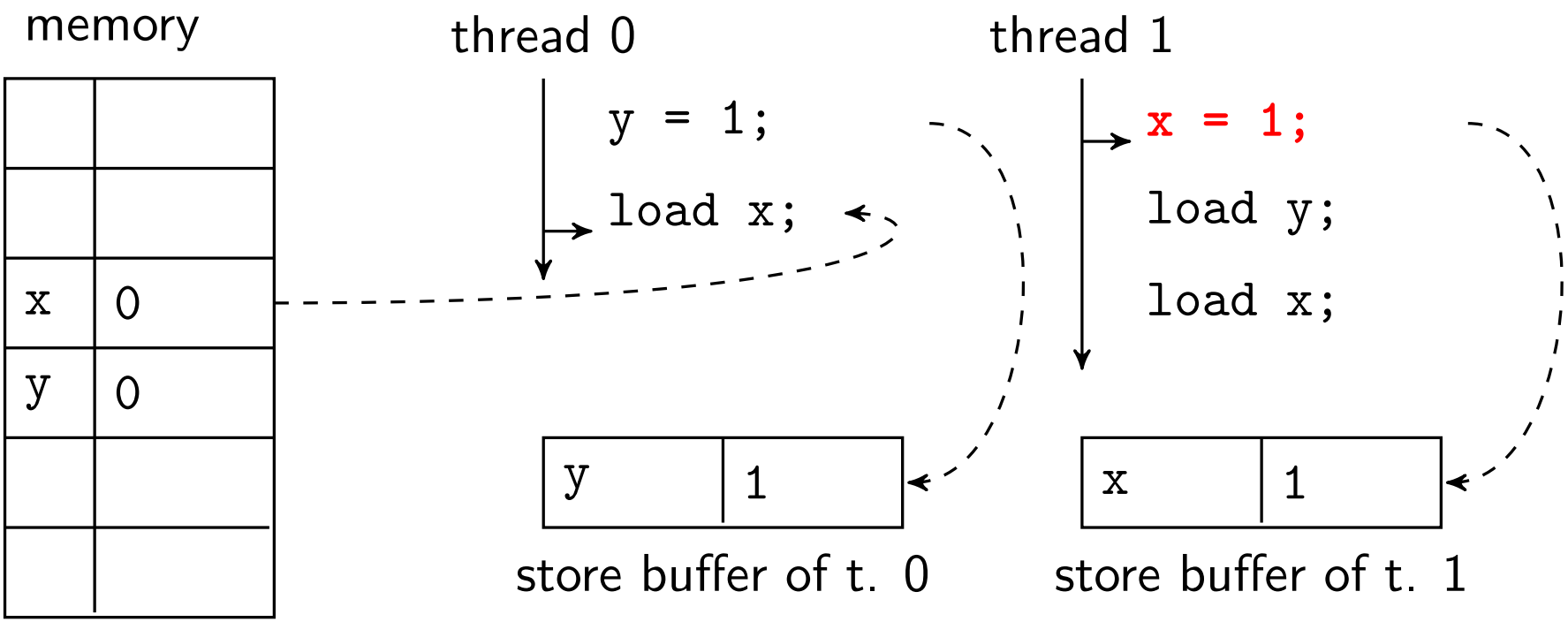

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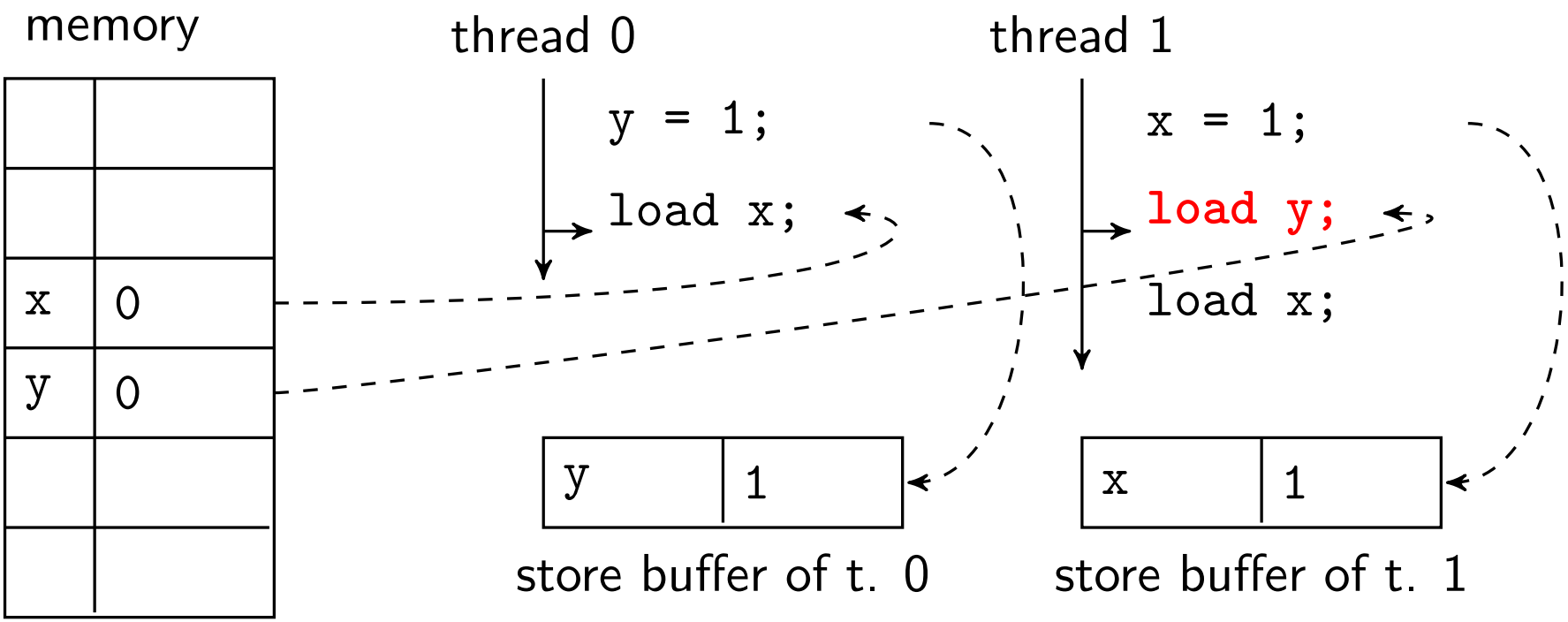

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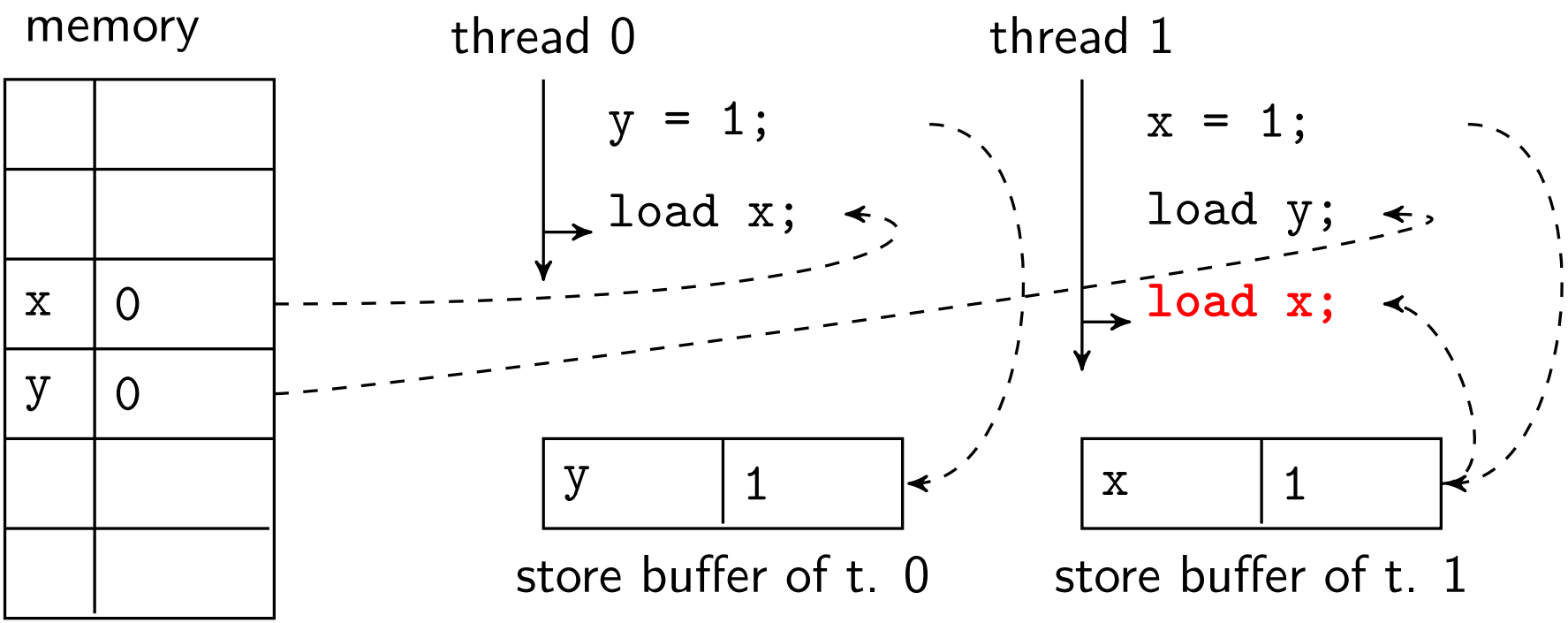

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thread 0

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store buffer of t. 0

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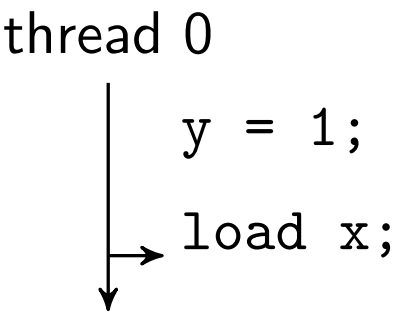
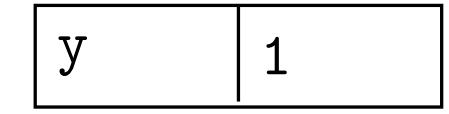
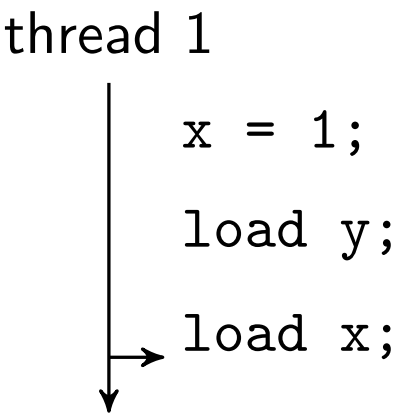




store buffer of t. 0



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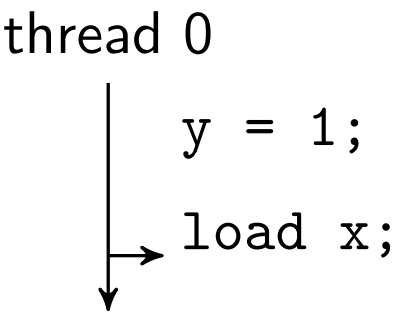

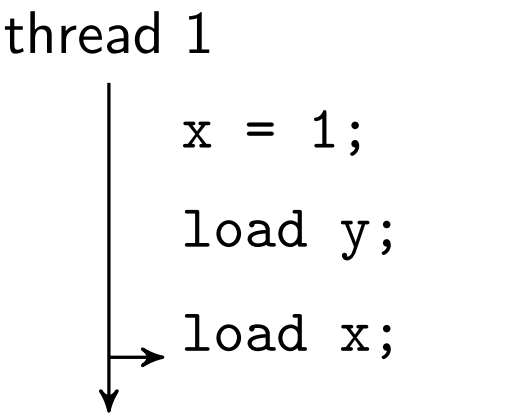

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- overall behaviour described by a **(relaxed) memory model**

- now: x86-TSO memory model
  - stores are performed to store buffer
  - core-local FIFO buffers
  - entries flushed eventually to the memory

Memory-Model-Aware Analysis I

- encode the memory model into the program
- verify it using a verifier without memory model support
  - e.g. DIVINE, a lot of other verifiers
  - program transformation instead of modification of the verifier

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x = 1;
int a = y;
```

$\rightsquigarrow$

```
_store( &x, 1 );
int a = _load( &y );
```

- `_load`, `_store` simulate the memory model
- (more complex in practice)

Memory-Model-Aware Analysis II

program transformation

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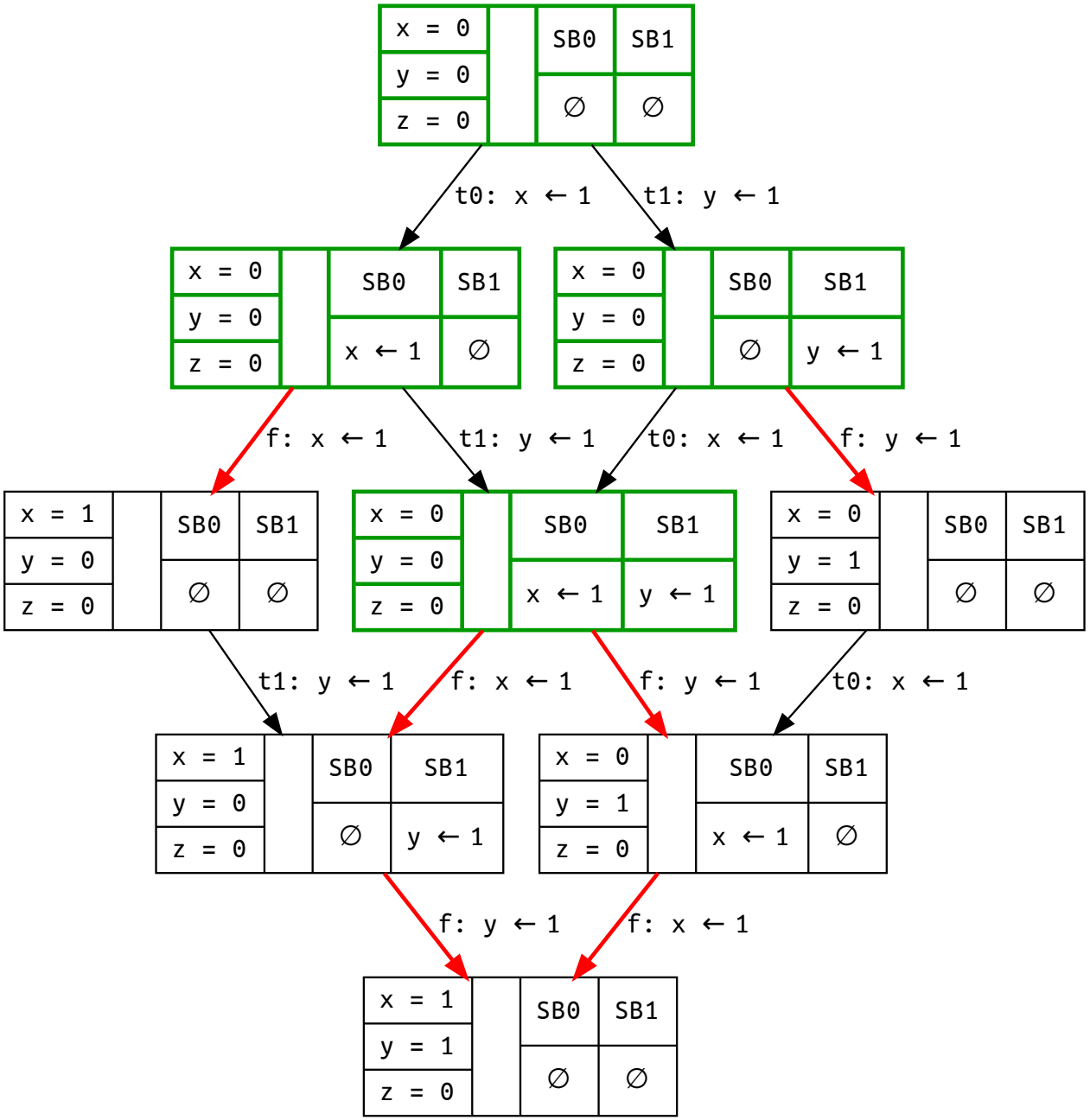
memory operations

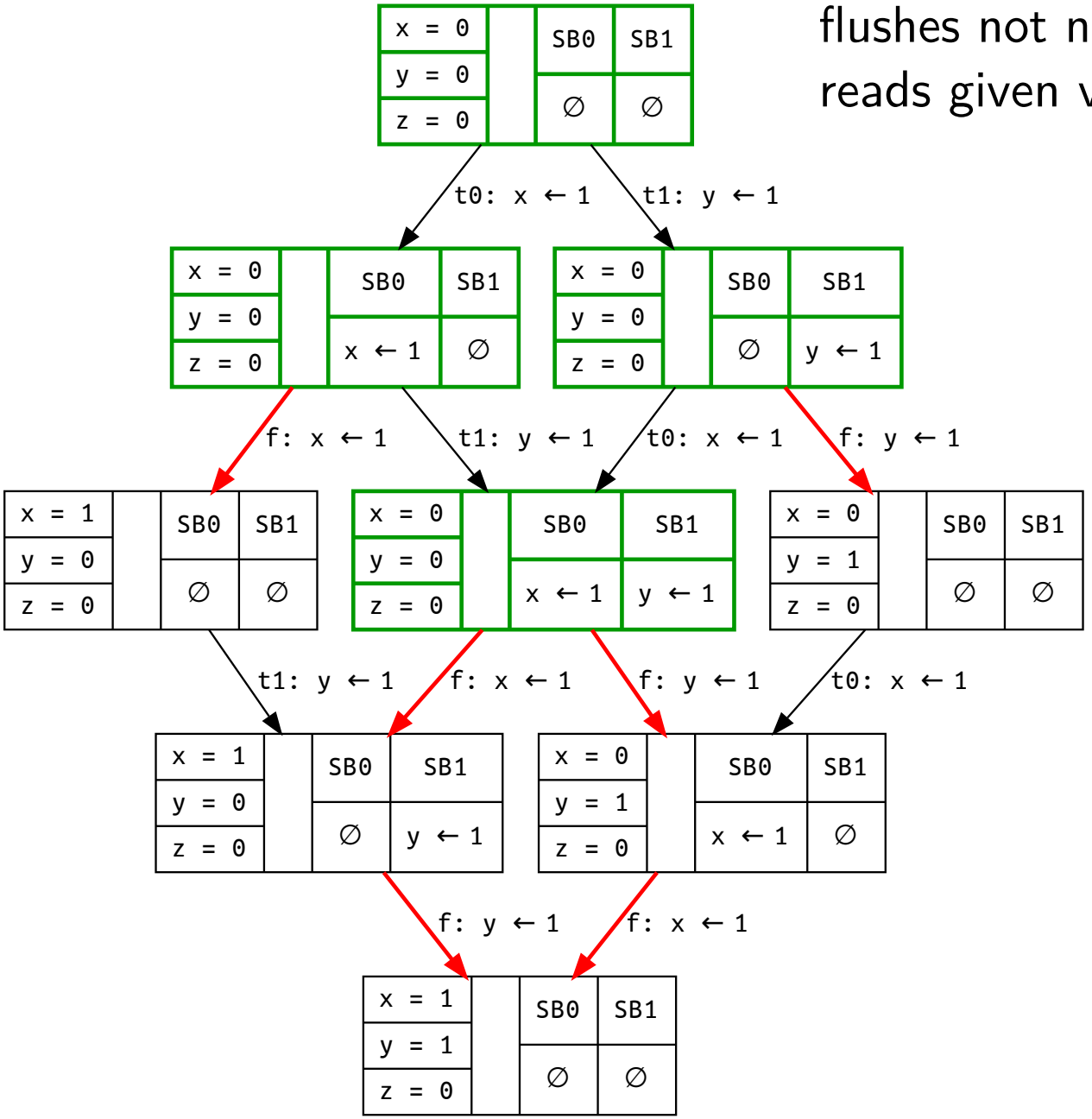
- memory model dependent
- rather complex (theoretically & technically)
- impact efficiency a lot $\rightarrow$ the main aim of my work
  - efficient data structures (time & memory)
  - amount of nondeterminism
- bounded reordering of (effects of) instructions

State Space Explosion



State Space Explosion

flushes not needed if noone reads given value



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- DIVINE's state space reduction uses these observations
- but relaxed memory simulation has to be adapted to support this

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- how to handle other entries in store buffer?
- memory barriers and compare-and-swap/read-modify-write not fully lazy
  - flushing of local store buffer can nondeterministically flush entries from other buffers
  - fully lazy barriers would show down DiOS

Lazy x86-TSO – Current Status I

the lazy simulation of x86-TSO store buffers mostly done

- one known missing corner case
  - in sequence of stores to unrelated addresses
  - solution will probably increase laziness and therefore performance
- probably some space for speed improvement

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current delays caused by interaction with state space reductions

- store buffers look like shared memory for reduction
- ensure reduction does not see every operation as visible
- not everything in memory model implementation can be hidden
  – “real” loads/stores

Lazy x86-TSO – Future

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2. add more tests and benchmarks
3. compare with other tools
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That is all... Thank You!